Device scaling in sub-100 nm pentacene field-effect transistors

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Reported here is the fabrication of 20–100 nm channel length pentacene field-effect transistors (FETs) with well-behaved current-voltage characteristics. Using a solution deposition method, pentacene grains span entire devices, providing superior contacts. Varying the gate oxide thickness, the effects of scaling on transistor performance is studied. When the channel length to oxide thickness exceeds 5:1, electrostatically well-scaled nanometer FETs are prepared. The results show that the device characteristics are dominated by the contacts. Decreasing the oxide thickness lowers the device turn-on voltage beyond simple field scaling, as sharper bending of the gate potential lines around the contacts more effectively reduces the molecule/source interfacial resistance. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2364154]

Organic semiconductors are important because they can serve as the active channels in field-effect transistors (FETs) for low-cost and flexible electronic applications.[1–4] Pentacene thin films have received the most attention due to their superior electronic properties relative to other thin film organic semiconductors.[5,6] Field-effect mobilities of $\sim 1\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ and current modulations greater than 10^6 are routinely achieved in micron-size devices, approaching the performance of amorphous silicon FETs. Previously, we reported a soluble precursor of pentacene that allows for solution processing while retaining pentacene's desirable electrical characteristics.[7] Moreover, this method provides devices that are exceedingly stable in air ambient at low operating powers.[8] In this letter, we study nanoscale pentacene FETs to understand the scaling required to increase the device speed and output current, lower the operating voltage, and reduce the likelihood of device degradation via thermal oxidation. In prior studies, nanoscale organic FETs were studied using vacuum deposited organic semiconductors. All, but one report,[9] show superlinear *IV* curves attributed to high resistance electrical contacts between the metal electrodes and the organic semiconductor.[10–22] In contrast, we report here that the solution method provides uniform thin film morphology for facile and reproducible fabrication of well-behaved nanoscale FETs and allows us to study the device scaling, electrostatics, and contact resistance.

The device structures, shown in Fig. 1, are fabricated by thermally growing 3, 5, or 10 nm of SiO_2 (t_{ox}) onto heavily *n*-doped silicon wafers that serve as the dielectric and gate of the transistors, respectively. Electron beam lithography is used to define 12 sets of source-drain electrodes (1 nm Ti/19 nm Au), with device channel lengths (L) ranging from 20 to 100 nm and widths (W) of 250 nm. To minimize the gate leakage, a 100 nm silicon oxide layer is e-beam evaporated to further insulate the large area contact pads from the gate. The large metal contact pads (10 nm Ti/190 nm Au) are then deposited onto the insulating layer so they make contact with the e-beam written electrodes. In the final fabrication step, 100 nm SiO_2 windows were defined to isolate the channel from the rest of the electrode structure. This ensures that the electrical current we measure is only due to the nanometer scale channels. The device structures are cleaned with acetone, methanol, and ethanol and further treated with an oxygen plasma. Pentacene is then deposited onto these devices by first spin coating the *n*-sulfinyl acetamide pentacene precursor and then annealing (200 °C in N_2 glovebox) by a procedure that has been previously reported.[7,8] The edges of the resultant devices are then cleaned to reduce device leakage. The transistor behavior was measured in air ambient using a probe station and parameter analyzer.

Figures 2(a) and 2(b) show the representative device characteristics for 20 and 60 nm channel length pentacene devices. The devices behave like long channel transistors

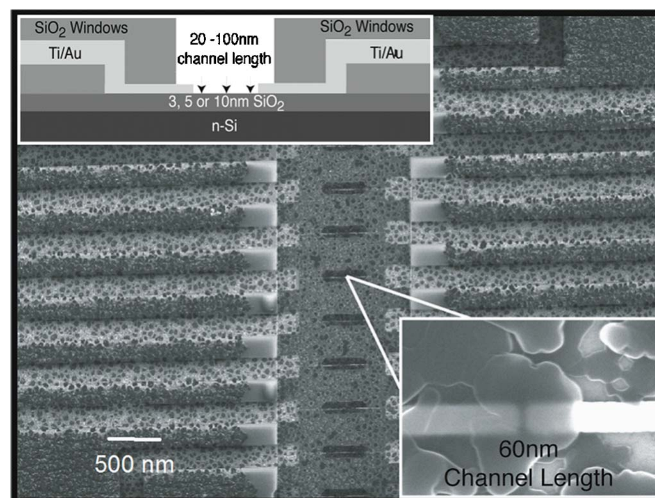

FIG. 1. Scanning electron microscopy (SEM) image of a set of pentacene field-effect transistors (top view). The top inset is a schematic cross section (not drawn to scale) of a single FET. The bottom inset is a SEM image of a 60 nm channel length device showing a single grain of pentacene spanning the gap.

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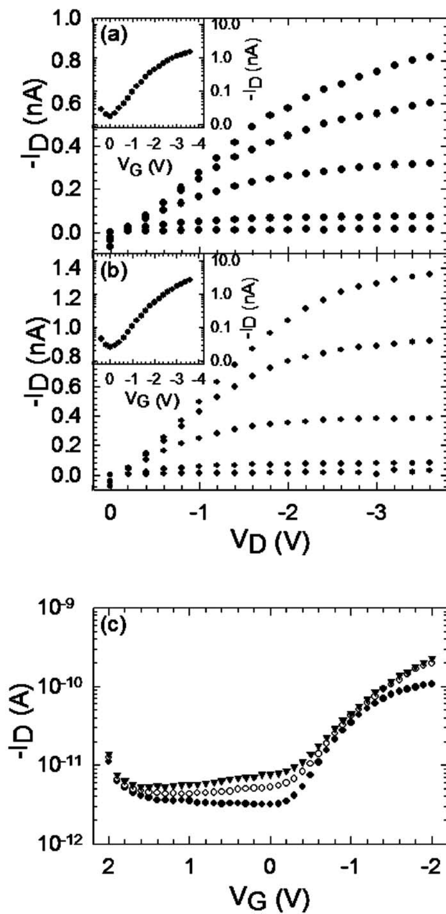

FIG. 2. Plot of $-I_D$ vs V_D and (inset) plot of $-I_D$ vs V_G (V_D scanned from 0 to –3.6 V and V_G scanned from 0 to –3.6 V) for (a) a 20 nm channel length pentacene FET with a 5 nm SiO_2 gate dielectric and (b) a 60 nm channel length pentacene FET with a 5 nm SiO_2 gate dielectric. (c) Plot of $-I_D$ vs V_G (V_G scanned from 2 to –2 V) for V_D of −1 V (closed circle), −1.5 V (open circle), and −2 V (closed triangle).

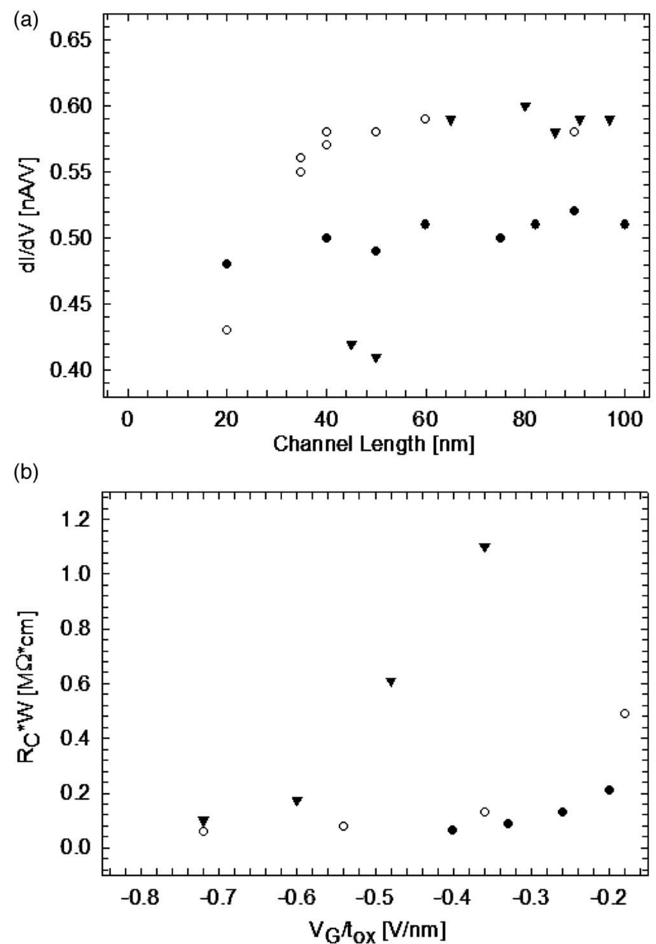

FIG. 3. (a) Plot of field-effect differential conductance (dI/dV) vs channel length for pentacene organic FETs with 3 nm (dark circles), 5 nm (open circles), and 10 nm (dark triangles) SiO_2 gate oxide thicknesses. Differential conductances are calculated from $I_D - V_G$ characteristics where V_G is scanned from 0 to −1.2 V at V_D=−1.2 V for the 3 nm gate oxide, V_G is scanned from 0 to −3.6 V at V_D=−3.6 V for the 5 nm gate oxide, and V_G is scanned from 0 to −7.2 V at V_D=−7.2 V for the 10 nm gate oxide. (b) Plot of the normalized contact resistance ($R_C W$) vs V_G/t_{ox} for SiO_2 thicknesses of 3, 5, and 10 nm. Device resistances are calculated in the linear regime from the slope of the $I_D - V_D$ characteristics where both V_D and V_G are scanned from 0 to −1.2 V for the 3 nm gate oxide, 0 to −3.6 V for the 5 nm gate oxide, and 0 to −7.2 V for the 10 nm gate oxide.

consisting of linear Ohmic regimes followed by current saturation at higher source-drain voltages. The transfer characteristics reveal a very low off current, equal to the gate leakage, with an I_{on}/I_{off} of 10^2. Most previous reports of nanoscale organic FETs fabricated by vacuum deposition of organic semiconductors have nonideal $I-V$ characteristics, showing superlinear behavior and a lack of current saturation.[10–22] This has also been seen in micron scale devices at low source-drain voltages and is known as current crowding.[20] The superlinear behavior is a result of the contacts behaving as "Schottky" barriers limiting charge injection from the source electrode to the semiconductor.[17,22–25] Vacuum deposited organic semiconductors show drastically different morphologies on the metal electrode surface and the surface of the gate dielectric.[9,21] One would expect the contact resistance to be larger in vacuum deposited devices. The effect of this difference in growth becomes magnified as the channels become smaller to the point that the grains become exceedingly small and do not span the nanometer scale devices. As shown in Fig. 1 (bottom inset), the solution-based deposition route yields a uniform morphology across the channel and source/drain contacts. While the $I-V$ characteristics are well behaved, the device resistance is still dominated by resistance at the contacts. The contact resistance, unreported in previous vacuum deposited nanoscale organic devices, is comparable to micron scale devices.[20] We have previously shown that the contact resistance may further be reduced by chemically modifying the contacts with a thiolated pentacene derivative.[22]

Figure 2(c) shows the drain current versus gate voltage at fixed source-drain voltage for a device with a 60 nm channel length and a 5 nm SiO_2 gate dielectric. The plot clearly shows p-type behavior of the devices as the drain current increases with increasing negative gate voltages and remains off at positive gate voltages. The curves are shifted to the left as the source-drain voltage is made increasing negatively. This suggests that increasing the source-drain voltage reduces the device contact resistance.[17,23] This is indicative of contact dominated devices where the output characteristics are limited by charge injection rather than the channel resistance.[17,23] In such devices, the source-drain voltage not only drives charge across the channel but can modulate the contact resistance to lower the injection barrier.

In order to separate the device electrostatics from the contact resistance, the gate oxide thickness was varied from 3 to10 nm. In Fig. 3(a), the differential conductance, calcu-

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lated from the slope of the I_D vs V_G curves in the saturation regime (high V_D), is plotted versus channel length for all oxide thicknesses. We plot differential conductance instead of mobility because these devices are dominated by contact resistance, whereas mobility is used to describe charge diffusion across the channel. At larger channel lengths, the differential conductance is constant with channel length, consistent with a contact dominated device. This is in agreement with our previous studies, where the device resistance was shown to be channel length independent arising from resistance of the contacts.[22] Significant loss of current modulation was observed in both the 5 and 10 nm gate oxide devices as the ratio of channel length to oxide thickness dips below 5:1. In the 3 nm gate oxide devices, no degradation is observed down to the 20 nm channel lengths measured as $L:t_{ox} > 5:1$ criterion. The fabrication of high quality thin dielectric films and the consideration of proper device scaling are important in studying nanoscale organic FETs.

Figure 3(b) is a plot of normalized contact resistance ($R_C W$) versus the gate voltage divided by the gate oxide thickness (V_G/t_{ox}) to scale the applied gate fields. The device resistances are calculated from the slope of the I_D vs V_D curves in the linear regime. The contact resistance at each V_G for each oxide thickness is found by extrapolating the linear dependence of R_C versus channel length to zero channel length. As expected, for a given t_{ox}, the total resistance decreases with increasing V_G/t_{ox} and then plateaus at higher values of V_G/t_{ox} as the gate potential decreases the barrier at the contacts. When comparing the three plots, a striking feature is that the contact resistance is lower for thinner gate oxides, even where V_G/t_{ox} is equivalent. The thinner the gate oxide, the more effective the field is per unit thickness of gate oxide. This is due to the shape of the gate constant potential lines of the devices. As the gate is brought closer to the semiconducting channel, the potential lines bend more sharply around the contacts causing more effective reduction of the metal-molecule barrier, more substantially lowering the contact resistance.[24,25] It is important to note that in the 3 nm gate oxide devices, the applied gate field was limited to 0.4 V/nm as higher applied fields lead to leakage and breakdown of the dielectric. The inability to operate the devices at higher gate fields leads to a lower maximum conductance [Fig. 3(a)] even though the contact resistance is actually lower.

In conclusion, we readily and reproducibly fabricated well-behaved sub-100 nm pentacene FETs using a solution deposition process. The improved morphology that allows individual grains to span the electrodes creates superior contacts compared to vacuum deposited pentacene in nanoscale organic FETs and provides motivation to develop alternative solution processable materials. This letter considers proper device scaling in nanoscale organic FETs. At ratios of channel length to oxide thickness greater than 5:1 maximum current modulation was attained. The nanoscale organic FET's performance is dominated by the contact resistance, as opposed to the device channel. The contact resistance present at the source/molecule interface was reduced by applying higher drain and gate voltages. As the gate oxide is thinned, the gate more effectively reduces the barrier at the source/molecule interface due to sharper contour of the potential lines at the contacts.

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